set of assignable locations in said container signal, locations to include adaptive stuff bits, where said set of assignable locations comprises a significant fraction of the locations within said container signal".

Regarding claim 3, the Office Action states it is unclear what is meant by a 'synchronous tributary". This rejection is moot as we have amended the claim to claim another feature of the invention. However, regarding possible interpretation of this patent, we state for the record that such a term is known to a person skilled in the art and no surrender of equivalents for other claims is intended.

Referring to claim 6, it is submitted that a person skilled in the art would understand that the phase difference between the two rates is the phase difference between the signals having the two rates. However the claim has been reworded for ease of readability. No surrender of scope is intended. Indeed, if anything, the reworded claim is broader in scope rather than narrower in scope than the original claim.

Referring to claim 7, the Office Action states that the terminology "substantially larger" renders the claim indefinite. While we disagree, the claim has been amended by deleting the word substantially and replacing it with significantly, as this amendment does not change the meaning of the claim, or surrender scope. As stated above with reference to claim 1, it is submitted that this language is clear and definite, and will be understood by a person skilled in the art. In addition to amending claim 7, we have also added a new set of claims 21-28 which uses different language, and includes the limitation:" mapping said continuous digital signal into said container signal by assigning from a set of assignable locations in said container signal, locations to include adaptive stuff bits, where said set of assignable locations comprises a significant fraction of the locations within said container signal".

Referring to claim 8, "reminder" was a simple typographical spelling error, and has been corrected.

It is submitted that the rejection Claim 13 should be an objection and not a rejection. Claim 13 has been broadened to remove the receiving step, which, incidentally, answers the alleged unclearness of the claim.

Accordingly, withdrawal of the s112 rejections to all of the rejected claims is solicited.

Accordingly, Claims 6-11 and 13-18 are now allowable.

The rejection under s. 3 of the Office Action, wherein claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sherman in view of Urbansky, is traversed as follows.

Sherman in general, and the cited passage in particular discloses transmitting signals of a fixed rate and interleaving 28 VT1.5s into an STS-1 frame. The mapping technique described is conventional and Sherman is an example of the prior art described in the background section of the present invention (see pp 2- 3 in general) and the following subsection in particular:

> As such, an STS-1 has a bit rate of 51.840 Mb/s. Lower rates are subsets of STS-1 and are known as virtual tributaries (VT), which may transport rates below DS3.... Higher rates, STS-N, where N=1, 3, 12, ...192 or higher, are built by multiplexing tributaries of a lower rate, using SONET add/drop multiplexers. An STS-N signal is obtained by interleaving N STS-1 signals. For example, an STS-192 is made of 192 STS-1 tributaries, each separately visible, and separately aligned within the envelope. The individual tributaries could carry a different payload, each with a different destination. ...
>
> Mapping of one rate or format into another is well known. Bellcore TR-0253 describes in detail the standard mappings of the common asynchronous transmission formats (DS0, DS1, DS2, DS3, etc) into SONET. Similar mappings are defined for the ETSI hierarchy mapping into SDH. Optical transmission equipment has mapped one proprietary format into another. For example, FD-565 could carry Nortel's FD-135 proprietary format as well as the DS3 standard format.
>
> However, the standards or proprietary schemes allow transportation of a very specific set of signals, with format specific hardware. These methods of mapping cannot be used to map rates that vary significantly from the standard. Furthermore, these mappings are each precisely tuned for a particular format and a particular bit-rate, with e.g. a ±20ppm tolerance. If a signal has, for example, a bit rate even 1% different than that of a DS3,

> cannot be transported within SONET. In addition, a different hardware unit is generally required to perform the mapping of each kind of signal.

Sherman does not describe the system as claimed. The system described in Sherman can only transmit a specific set of signals as described above and can not transmit a signal with an arbitrary rate R1.

Furthermore, as admitted by the examiner, Sherman does not teach or suggest the claimed invention wherein the invalid locations are uniformly interspersed across the frame. The Official Action than states that:

> "However, Urbansky discloses a system for justifying signals with variable rates wherein stuff bits are uniformly distributed (see column 2). It would have been obvious to one skilled in the art at the time of the invention to uniformly distributed the invalid time slots, wherein the stuffing bits are stuffed, as taught by Urbansky, in the system of Sherman because if the stuffing bits are non-uniformly distributed it will lead to jitter problems when the signal is de-multiplexed, as Urbansky points out in column 1, lines 6-8."

It is submitted that this is an improper basis for rejecting the claim, as the Office Action effectively uses the claimed invention to piece together prior art references to achieve the claimed invention, and uses one of the advantages described in the present application as the motivation to combine.

For one thing, the Urbansky reference predates the filing date of the Sherman reference by approximately 5 years (which is a very long time in this art). This begs the question that if this was obvious, why was this not suggested within the Sherman reference itself?

The Office Action states it would have been obvious to combine the these references to achieve the advantage stated, but the simple fact is, prior to the present invention, this was not known, nor was it known how to achieve this result.

Furthermore, the Sherman reference teaches a transmission network and not a specific circuit as described in Sherman.

Furthermore, even if the above is not a sufficient basis for traversing the rejection, it is submitted that it would not have been obvious for a person skilled in the art to look at the circuit taught by Urbansky because Urbansky is directed to solving a the problem of inserting stuff bits at predetermined locations in a parallel bit stream of eight parallel bits. (see Urbansky, column 5, lines 64-66, which is immediately above the passage cited in the Office Action). Accordingly, this does not lead to the claimed invention, which maps a signal capable of having any arbitrary rate R1 (less than the rate R).

Accordingly, it is submitted that rejection to claim 1 is traversed, and withdrawal of the rejections to claim 1 (and consequently claims 2-5 and 12) is requested.

New claims 21 is certainly allowable over the cited art, as neither reference, either separately or combined teach mapping said continuous digital signal into said container signal by assigning from a set of assignable locations in said container signal, locations to include adaptive stuff bits, where said set of assignable locations comprises a significant fraction of the locations within said container signal.

Accordingly, it is submitted that all of claims 1-28 are allowable (claims 19-20 are already allowed).

Respectfully Submitted,

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: ROBERTS, Kim B.

Serial No: 09/349,087 Art Unit: 2662

Filed: July 8, 1999 Examiner: Odland, David E.

Subject: MAPPING ARBITRARY SIGNALS INTO SONET

**MARKED UP VERSION OF THE SPECIFICATION**

According to *AMENDMENTS IN A REVISED FORMAT NOW PERMITTED* as stated in the United States Patent and Trademark Office letter dated February 20, 2003

**Page 1, line 4, delete:**

"BACKGROUND OF THE INVENTION"

**Page 1, change the title of paragraph 2 to:**

--Background of the Invention--

**Page 3, Paragraph 4 beginning on line 29 and ending at line 32;**

A1

It is known to have a packet or cell based [United States Patent No. 5,784,594 (Beatty) purposes of "TDM Wrapper"] format where an arbitrary signal is mapped into as much of a frame as required, and the rest of the frame is left empty. However, this method requires a very large memory for each direction of conversion to hold the bits while waiting for the

**Page 8, Paragraph 4 beginning on line 18 and ending at line 20;**

A2

On the other hand, the number of stuff bits necessary to fill the block field 8 varies as a function of the rate *R1* of the continuous format signals *S1*. These stuff bits are called herein adaptive stuff bits.

**Page 8, Paragraph 5 beginning on line 21 and ending at page 9, line 2;**

A3

According to the invention, the adaptive stuff bits are added to the data bits of the signal *S1* [are] and mapped into frame 1 [with evenly interspersed fixed stuff bits and adaptive stuff bits. These stuff bits are distributed uniformly within each block.] on the fly, since the rate *R1* may not be known in advance. Therefore, the

synchronizer defines a valid location, that is a location for a data bit, and an invalid location, that is a location for a stuff bit for the next block, based on phase information accumulated when the data bits of the current block are mapped. In addition, the synchronizer also distributes evenly the overhead bits at the time of the actual mapping, but realigns these in the timeslots provided according to the SONET standard after mapping operation, so that the frame is recognized by the SONET equipment. At the far end, the synchronizer effects the reverse operation, by absorbing the fixed stuff bits and the adaptive stuff bits, so that the data bits can be reverse-mapped to regenerate *S1*.

Cont #3

**Page 9, Paragraph 1:**

It is to be noted that Figure 1B shows the structure of a frame intuitively; in accordance with this invention the mapping algorithm distributes the [fixed stuff] data bits and the adaptive stuff bits uniformly within the frame 1. We also note that the above calculations are applicable to a STS-192c frame; similar consideration apply to other SONET signals.

A4

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

IN RE APPLICATION OF: ROBERTS, Kim B.

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**MARKED UP VERSION OF THE CLAIMS**

According to *AMENDMENTS IN A REVISED FORMAT NOW PERMITTED* as stated in the United States Patent and Trademark Office letter dated February 20, 2003

**I CLAIM**

SUB B1

1. (Currently Amended) A method for transmitting a continuous digital signal of an arbitrary rate R1 over a synchronous network ~~as a transparent tributary,~~ comprising:

selecting a fixed length container signal of a rate R, where R is higher than said arbitrary rate R1 of said continuous signal; and

at a transmit site, distributing the bits of said continuous signal into valid ~~timeslots~~ locations of a frame of said container signal and providing stuff bits into invalid ~~timeslots~~locations,

A5

wherein said invalid ~~timeslots~~ locations are uniformly interspersed across said frame.

2. (Original) A method as claimed in claim 1, wherein said container signal is a SONET/SDH signal, and said synchronous network is a SONET/SDH network.

3. (Currently Amended) A method as claimed in claim 2, wherein said continuous digital signal is also a SONET/SDH signal ~~further comprises a synchronous tributary~~.

4. (Original) A method as claimed in claim 2, wherein said SONET/SDH signal comprises a plurality of transparent tributaries.

5. (Currently Amended) A method as claimed in claim 1, wherein said ~~invalid timeslots~~stuff bits comprises ~~one of a~~ fixed stuff and ~~an~~ adaptive stuff bits.

6. (Currently Amended) A method as claimed in claim 5, wherein said step of distributing comprises:

~~receiving a continuous stream of data bits and~~ determining the phase difference between said ~~arbitrary rate R1~~continuous digital signal and said ~~rate R~~container signal;

adding to the bits of ~~to~~ said continuous digital signal including ~~stream~~ a definite number of ~~timeslot~~locations for accommodating said fixed stuff bits within said frame, and an adjustable number of ~~timeslot~~locations for accommodating said adaptive stuff bits within said frame~~,~~ based on said phase difference.

Cont A5

7. (Currently Amended) A method as claimed in claim 6, wherein said adjustable number is ~~substantially~~significantly larger than said definite number.

8. (Currently Amended) A method as claimed in claim 6, wherein said definite number includes transport overhead (TOH) ~~timeslot~~locations and ~~reminder~~ remainder fixed stuff bits ~~timeslot~~locations.

9. (Currently Amended) A method as claimed in claim 8, further comprising providing maintenance, operation, administration and provisioning information in said TOH ~~timeslot~~locations.

10. (Currently Amended) A method as claimed in claim 6, wherein said step of adding comprises:

partitioning said frame into a number of equally sized data blocks and said definite number of ~~timeslot~~locations;

for each block,

~~determining the number of fixed stuff bits and evenly distributing said fixed stuff bits within said block;~~

determining a control function β indicative of said adjustable number; and

~~evenly mapping said fixed stuff bits and~~ adding said adaptive stuff bits ~~uniformly within a next block~~ based on said control function.

11. (Currently Amended) A method as claimed in claim 10, wherein said step of mapping comprises:

providing a counter C for identifying a ~~timeslot~~location in said block;

defining the binary bit reversal α of said control function

calculating the bitwise transition delta of said counter C; and

determining if a ~~timeslot~~location identified by said counter C is an invalid ~~timeslot~~location, whenever a function Valid (C, β) is false; and

providing an adaptive stuff bit into said invalid ~~timeslot~~location.

12. (Currently Amended) A method as claimed in claim 1, further comprising recovering said continuous signal from said synchronous signal at a receive site, by extracting the data bits of said continuous signal from said valid ~~timeslot~~locations of said frame.

CONT A3

13. (Currently Amended) A synchronizer for mapping a continuous format signal of an arbitrary rate for transport over a synchronous network as a transparent tributary signal, comprising:

a data recovery unit for ~~receiving said continuous format signal and~~ recovering, from said continuous format signal, a stream of data bits and a data clock indicative of said arbitrary rate;

a receiver buffer unit for receiving said stream of data bits, determining a phase difference between said arbitrary rate and the rate of a frame of said tributary, and generating a control function β;

a mapping unit for extracting said stream of data bits from said receiver buffer unit at a mapping clock rate, and ~~uniformly distributing a count of~~inserting stuff bits and said data bits into said frame at a block clock rate according to said control function β.

14. (Currently Amended) A synchronizer as claimed in claim 13, wherein said receiver buffer unit comprises:

an elastic store for temporarily storing an amount of data bits of said stream at said data rate clock and providing said data bits to said mapping unit at said block clock rate;

a digital PLL for determining the phase difference between said arbitrary rate and said mapping clock and providing said control function β.

15. (Original) A synchronizer as claimed in claim 13, wherein said data recovery unit comprises a frequency agile PLL for detecting said arbitrary rate, and a receiver for detecting said data bits using said data clock.

16. (Currently Amended) A synchronizer as claimed in claim 13, wherein said mapping unit comprises:

a block clock gapper for receiving a clock indicative of the rate of said synchronous frame and providing said block clock of a block rate accounting for all ~~timeslots~~locations of said synchronous frame and with ~~gapps~~ gaps accounting for a definite number of ~~timeslots~~locations for accommodating fixed stuff bits;

a mapping clock gapper for receiving said block clock and said control signal β and providing a mapping clock of a mapping rate accounting for all ~~timeslots~~locations of said synchronous frame and with ~~gapps~~ gaps accounting for an adjustable number of ~~timeslots~~locations for accommodating adaptive stuff bits within said frame; and

a mapper for receiving said block clock and said mapping clock and accordingly mapping said stream of data bits in said frame.

CONT A5

17. (Currently Amended) A synchronizer as claimed in claim 13, further comprising a receiver OH FIFO for re-arranging a plurality of transport overhead TOH ~~timeslots~~locations for seamless transport of said frame within said synchronous network.

18. (Currently Amended) A synchronizer as claimed in claim 17, further comprising an overhead multiplexer for adding operation, administration, maintenance and provisioning data into said TOH ~~timeslots~~locations.

19. (Original) A de-synchronizer for reverse mapping a continuous format signal of an arbitrary rate received over a synchronous network as a transparent tributary signal, comprising:

a reverse mapping unit for receiving a frame of said tributary at a block clock rate and a control function β and extracting a stream of data bits at a mapping clock rate, while excluding stuff bits according to said control function β;

a transmitter buffer unit for receiving said data bits, and determining a phase difference between said arbitrary rate and the rate of said frame; and

a data transmit unit for receiving said data bits and transmitting said continuous format signal at a data rate controlled by said phase difference.

20. (Original) A de-synchronizer as claimed in claim 19, wherein said control function β is received in said frame.

21. (New) A method for transmitting a continuous digital signal of a rate R1 over a synchronous network comprising:

selecting a container signal of a rate R, where R is higher than said rate R1 of said continuous signal; and

mapping said continuous digital signal into said container signal by assigning from a set of assignable locations in said container signal, locations to include adaptive stuff bits, where said set of assignable locations comprises a significant fraction of the locations within said container signal.

CONT A5

22. (New) A method as claimed in claim 21, where the location and the number of stuff bits assigned depends on the phase of said continuous digital signal.

23. (New) A method as claimed in claim 22, wherein said step of mapping comprises:

assigning a definite number of locations as fixed stuff bits within a frame of said container signal, and an adjustable number of locations as said locations to include adaptive stuff bits within said frame.

24. (New) A method as claimed in claim 23, wherein said step of adding comprises:

partitioning said frame into a number of equally sized data blocks and said definite number of locations;

for each block,

determining a control function β indicative of said adjustable number; and

mapping data bits and said adaptive stuff bits within the block based on said control function.

25. (New) A method as claimed in claim 24, wherein said step of mapping comprises:

providing a counter C for identifying a location in said block;

defining the binary bit reversal α of said control function β;

calculating the bitwise transition delta of said counter C; and

determining if a location identified by said counter C is an invalid location, whenever a function Valid (C, β ) is false; and

providing an adaptive stuff bit into said invalid location.

26. (New) A method as claimed in claim 23, further comprising recovering said continuous signal from said synchronous signal at a receive site, by extracting the data bits of said continuous signal from said frame.

Cont A5

27. (New) A method as claimed in claim 24, wherein said phase is communicated to a far end receiver and wherein said far end receiver uses said phase to recover said continuous signal from said synchronous signal by extracting the data bits of said continuous signal from said frame.

28. (New) A method as claimed in claim 21 wherein said continuous signal is a SONET/SDH signal, said container signal is a SONET/SDH signal, and said synchronous network is a SONET/SDH network